Designing and Configuring Custom, Ultra-Low Power FPGAs

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Motivation: Low-power sensors in Ubiquitous Computing

- Requirements
  - Low Power/Energy Consumption
  - Substantial Processing Capability
  - Flexible Hardware
  - Low Development and Deployment Cost

https://encrypted-tbn1.gstatic.com/images?q=tbn:ANd9GcQCNBXqIdhnsSVYp4y1A4MnKeoVOVfLomVOqtyQT-wQRZij_sy7

http://www.valencell.com/blog/2013/12/wearable-technology-all-about-people

Current Options

- Build System w/ Commercial-Off-The-Shelf (COTS) parts
  - Flexibile, but too high power consumption and size
- Build ultra-low power (ULP) SoCs
  - Efficient and powerful, but inflexible

Problem – neither option of these options fulfill all of the requirements pervasive low-power sensing

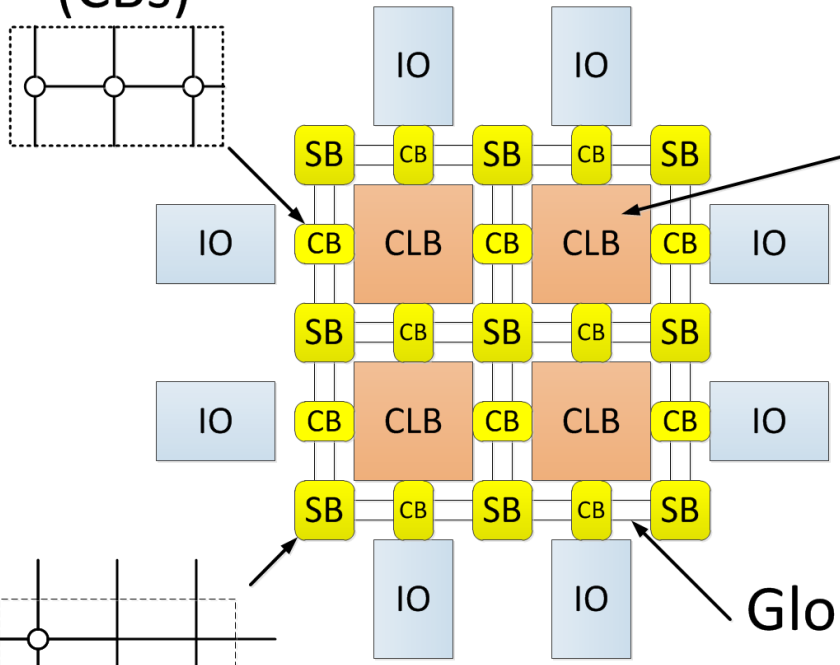
Solution – design of ULP Field Programmable Gate Arrays (FPGAs) for balance between efficiency and flexibility

Outline

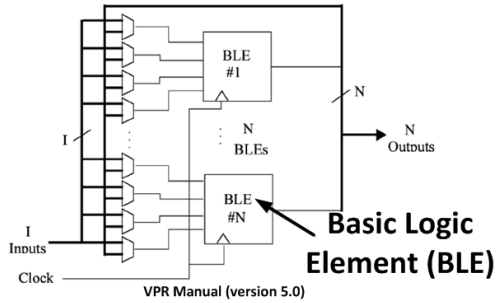
- Motivation
  - Ultra-Low Power FPGAs
  - FPGA Background
  - Custom-FPGA Design
- Thrust 1: FPGA Sub-Circuit Design Exploration
- Thrust 2: FPGA Architecture Re-examination
- Thrust 3: RCGC – Reconfigurable Circuit Generation and Configuration
- Thrust 4: Embedded FPGAs in ULP SoCs
- Timeline & Publications
- High Level Impact

FPGA Background

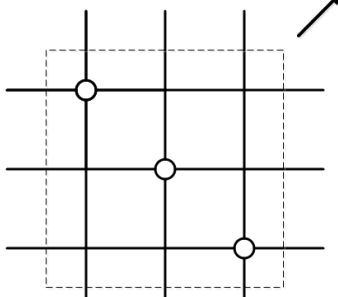
Connection Boxes (CBs)



Configurable Logic Blocks (CLBs)



Global Interconnect



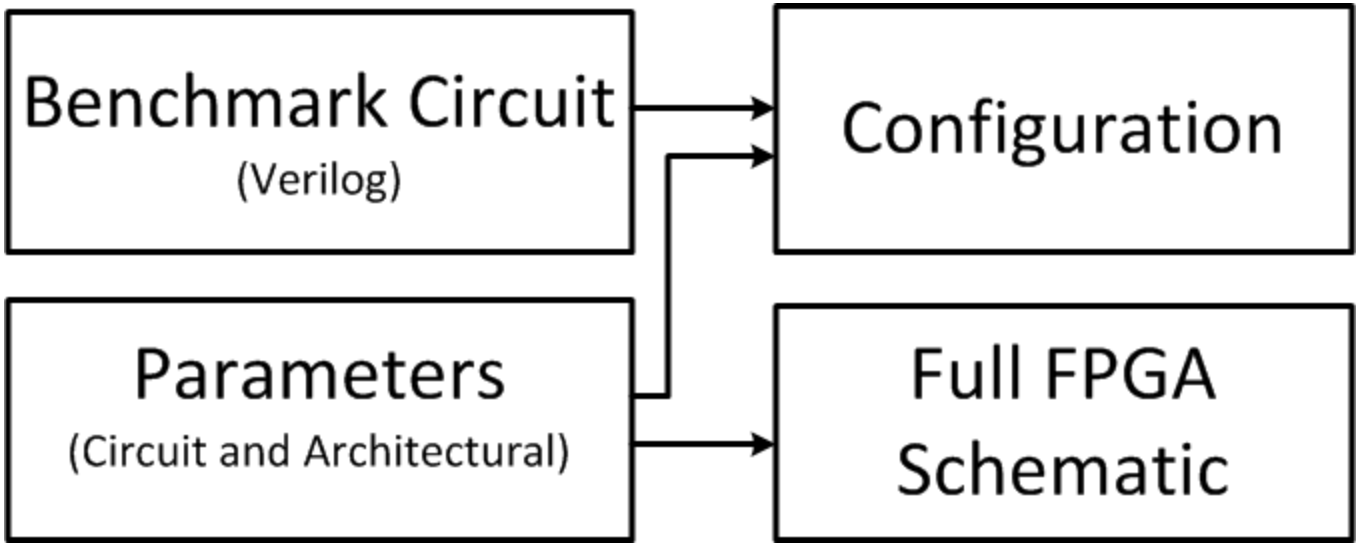
Switch Boxes (SBs)

Motivation – Custom-FPGA Design

- Circuit-level and architectural optimizations for ULP FPGAs need to be tested at the system-level
  - Build full FPGA schematic
  - Configure FPGA schematic
- Problems
  - Building FPGA schematics by hand is infeasible
    - # of transistors
    - # of design knobs
  - No tools for configuration
    - Commercial tools only work for specific hardware
    - Open-source tools are abstractions of FPGA mappings, not configuration bit locations (VTR)

Proposed Solution

- Toolflow – Reconfigurable Circuit Generation and Configuration (RCGC)
  - Generate schematics of FPGA fabrics
  - Generate configurations for schematics



Thesis Statement(s)

- ULP FPGAs combine efficiency, flexibility, and computing capability to create a single, low-cost platform for ULP applications.
- ULP FPGA fabrics can also serve as small IP-blocks to create flexibility and low-overhead testability in ULP SoCs.
- Extending FPGA mapping tools to generate configurations and schematics for custom-FPGA fabrics allow thorough design verification and validation.

ULP FPGAs in Industry/Academia

FPGA	Size (# of LUTs)	Power (µW)	Configuration Bit Topology	Frequency (MHz)
Lattice iCE40[1]	384-7680	Static: 21-250 Active: just ↓ 1k[7,8]	SRAM	275
Microsemi IGLOO nano[1]	100-3000	Static: 2 Active: 400[6]	Flash	160-250
Ryan et al [6][2]	1134	Static: ~35[3,4] Active: ~12.5[3,4]	5T-SRAM	~33[3]
Grossmann et al [7][2]	128	Static: 8.9 Active: 34.6	6T Latch	16.7
Tuan et al [8][2]	1500-15000	Static: 46-460 Active: 13k-130k	SRAM	244[5]

1. Commercial ULP FPGAs
2. Academic ULP FPGAs
3. Estimated from plots in the paper
4. Simulation result of 780 LUTs
5. Reported approx. 27% reduction from Xilinx Spartan-3
6. Obtained from Microsemi Power Calculator worksheet
7. Mid-range iCE40 model
8. From news article in EE times: Ultra-low power FPGAs enable always-on sensor solutions for context-aware mobile apps

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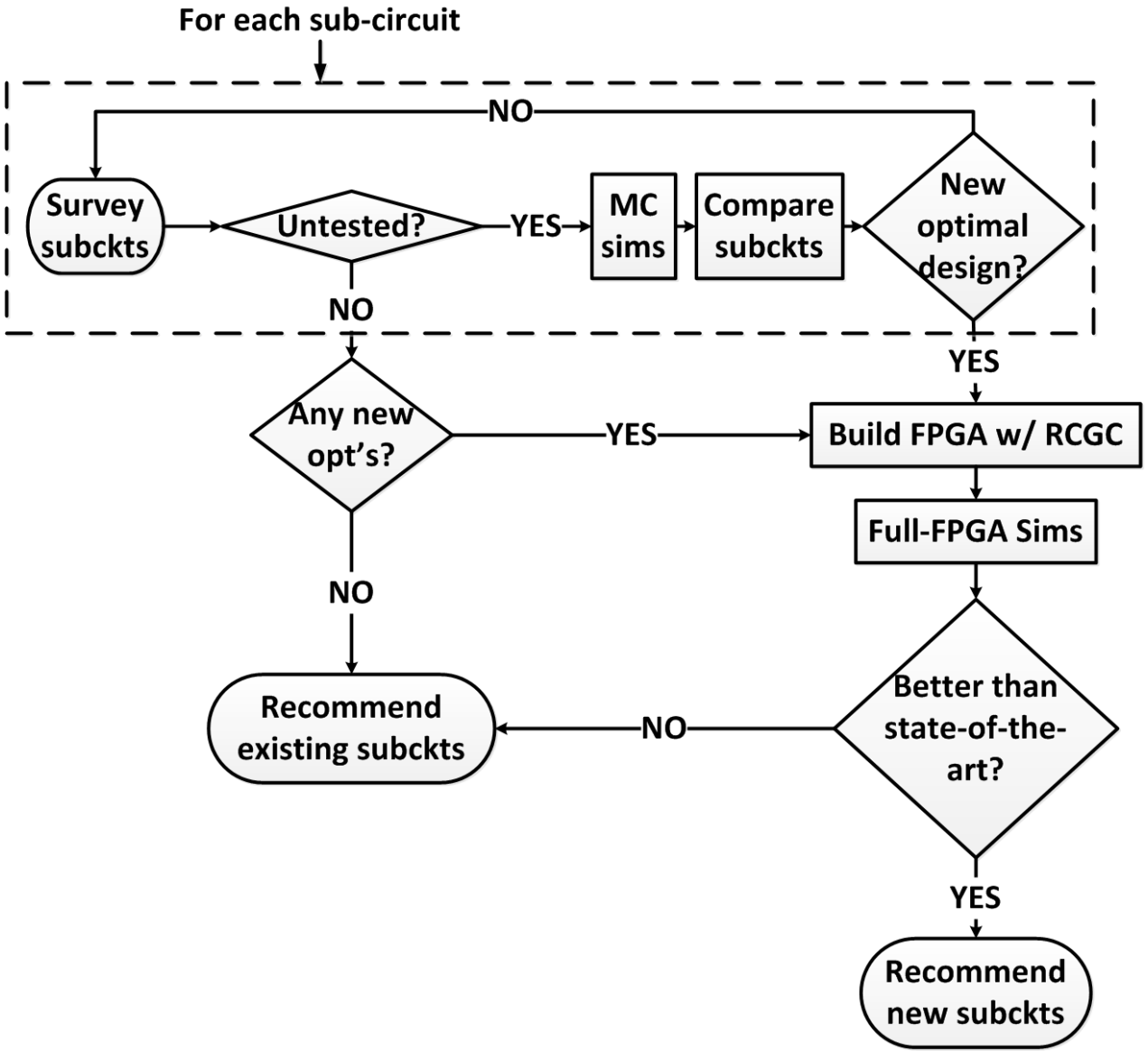
- Timeline
- Publications

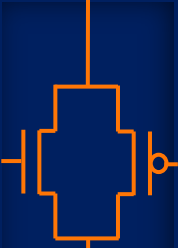
Motivation: FPGA Sub-Circuit Exploration

- **Problem:** FPGAs overlooked for ULP applications
  - High overhead for flexibility

- **Research Question:** How can we redesign the circuit elements in FPGAs to minimize power consumption, while still providing adequate functionality and performance for ULP applications?

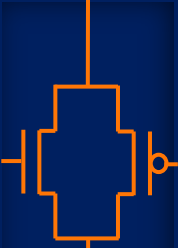
Approach:
FPGA Sub-Circuit Exploration





Knobs: FPGA Sub-Circuit Exploration

- Circuit topology
  - Routing switches: pass gate, buffer, etc.
  - CLBs: intra-CLB connectivity
  - Configuration bits: SRAMs, latches, etc.
- Operating voltage
- Transistor type
  - High V_T, etc.
- Transistor sizing
- Path length (for routing switches)

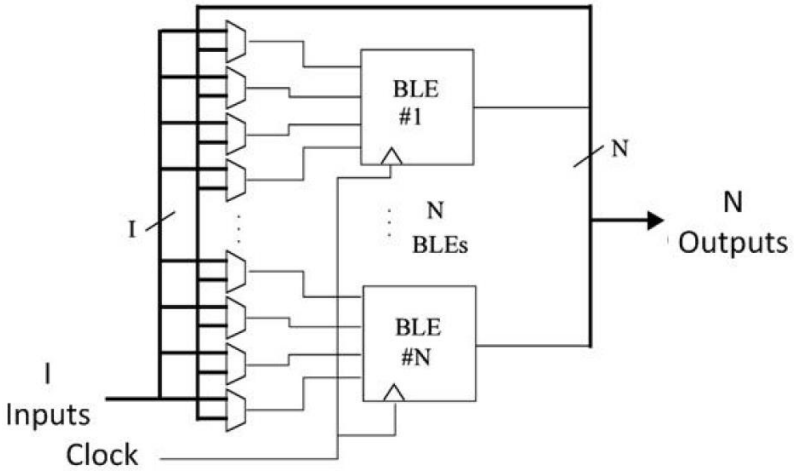


Metrics of Importance: FPGA Sub-Circuit Exploration

- Area
- Power consumption
- Energy consumption
- Robustness
  - Process, voltage, and temperature (PVT) variations
- Routeability (for CLBs)
- Hold Margin (for configuration bits)
- Retention Voltage (for configuration bits)

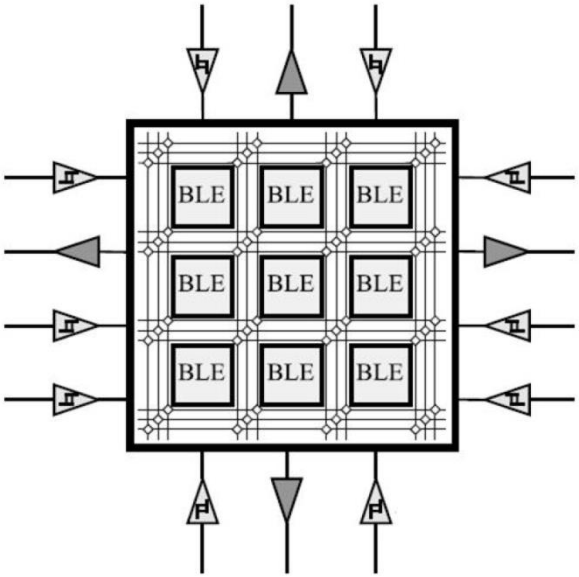
CLB Topology Exploration

- Mux-Based CLB
  - Standard practice for FPGAs
  - Knob – depopulation



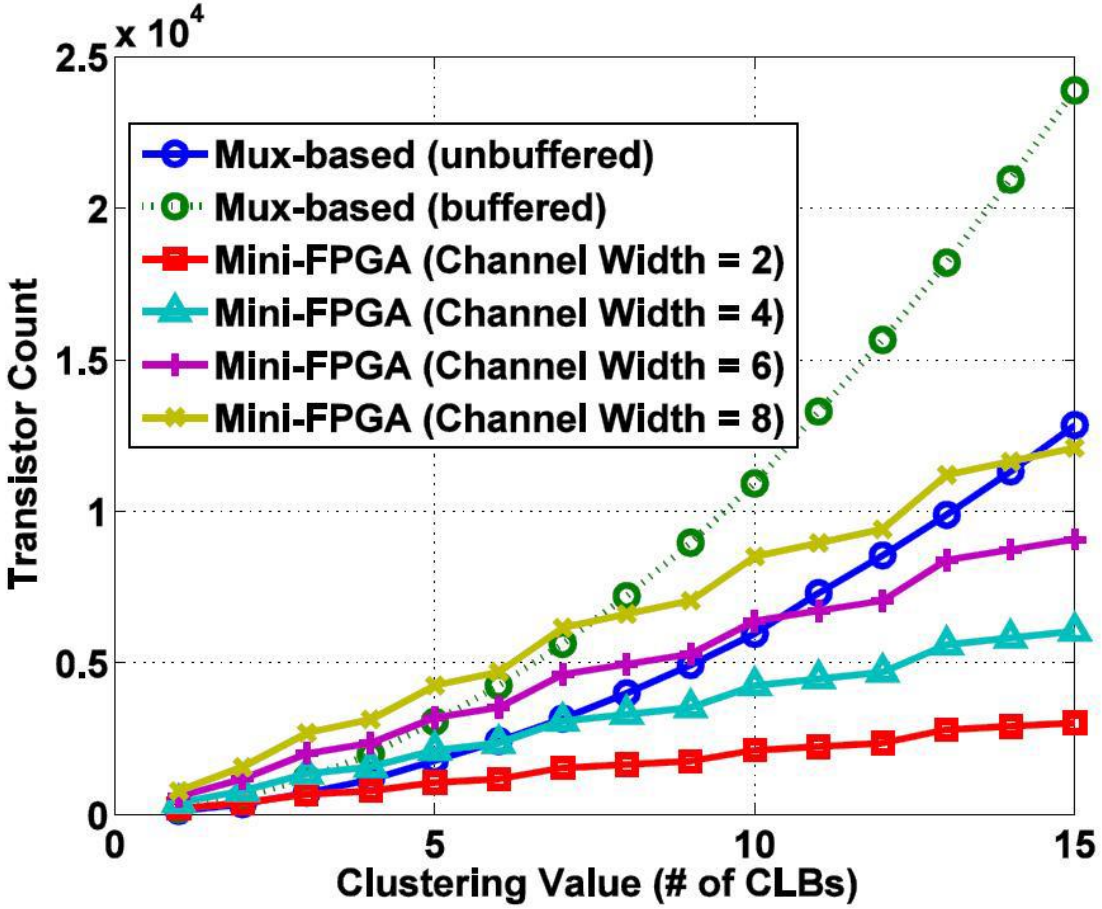
VPR version 5.0 manual

- Mini-FPGA CLB
  - Use FPGA-style connectivity for the CLB to connect BLEs
  - Knob – channel width



Ryan et al CICC '10

Preliminary Results: Area
CLB Topology Exploration



Small N - Mux-based CLBs minimize area

Large N - Mini-FPGA CLBs minimize area

Preliminary Results: Area
CLB Topology Exploration

Mini-FPGA vs. Mux (Buffered) - Break Even Points				
	K = 4			
Channel Width	**Break Even Points @ Different Depopulation %'s**			
	0%	50%	66%	75%
2	Always Less	N = 4	N = 5	N = 6
4	N = 3	N = 8	N = 11	N = 14
6	N = 6	N = 11	N = 16	N = 22
8	N = 9	N = 15	N = 23	N = 29
	K = 6			
2	Always Less	N = 2	N = 3	N = 4
4	N = 2	N = 4	N = 6	N = 8
6	N = 4	N = 6	N = 9	N = 12
8	N = 4	N = 9	N = 14	N = 16

Contributions: FPGA Sub-Circuit Exploration

- Survey of different techniques for design of FPGA sub-circuits for ULP operation
  - Configuration Bits
  - Routing switches
  - Configurable Logic Blocks (CLBs)
- Design space exploration across circuit-level and architectural knobs
- Recommendations for circuit-level optimizations for ULP FPGA design

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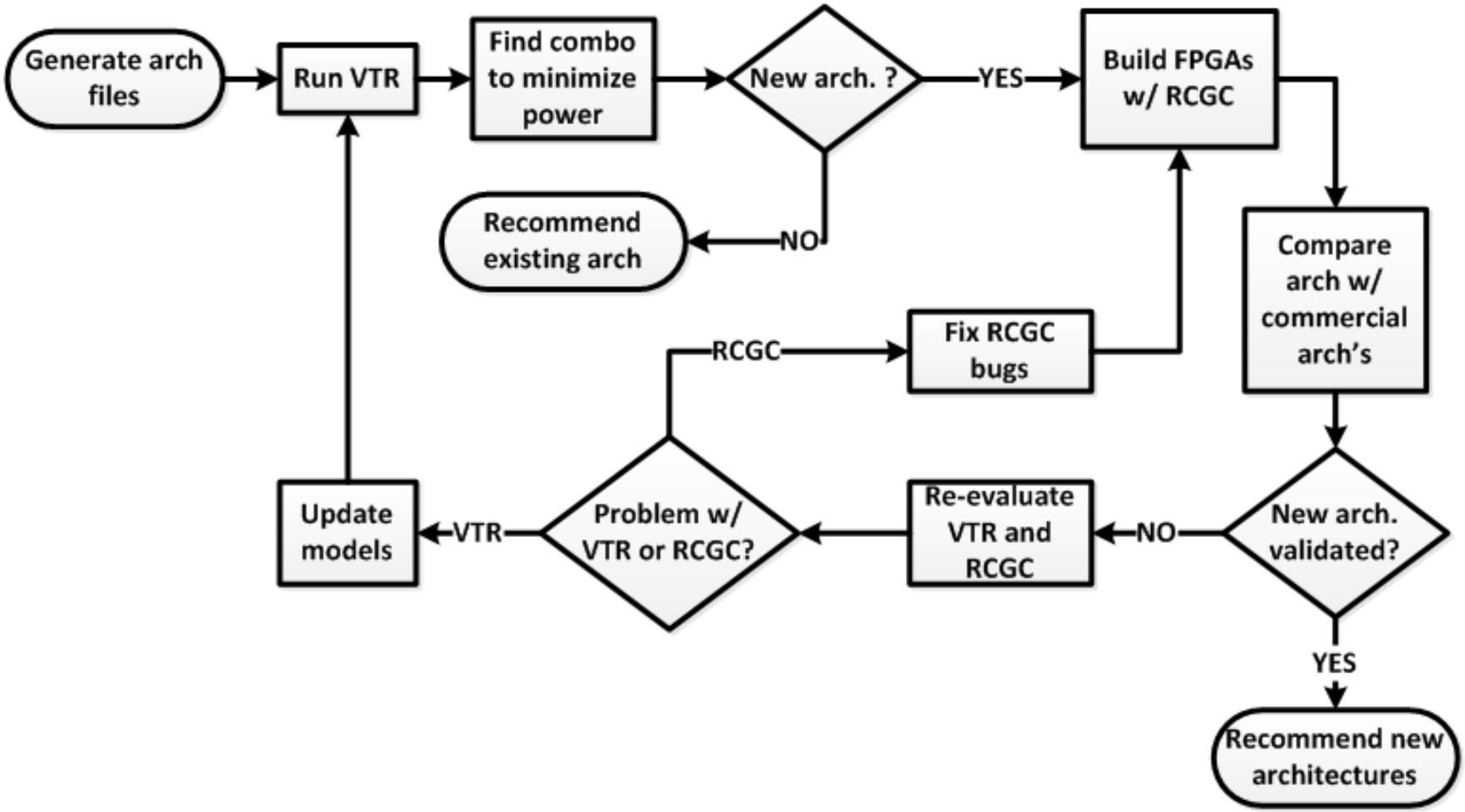
- High Level Impact

Motivation: FPGA Architecture Re-examination

- **Problem:** Driving force for FPGA design in industry is performance
  - GHz performance
  - ULP applications - Low performance requirements (kHz – MHz)

- **Research Question:** How does the optimal FPGA architecture change with a different set of primary metrics, namely area and power consumption?

Approach: FPGA Architecture Re-examination



Knobs: FPGA Architecture Re-examination

- Intra-CLB architecture (k, N)
- Channel width (W)*
- Channel Fanout (FC)
  - Different for CLB inputs, CLB outputs, and I/O blocks
- Segment Length (L)
  - Commercial FPGAs – distributions of L
- Uni- vs. bi-directionality of interconnect wires

Metrics of Importance: FPGA Architecture Re-examination

- VTR Exploration
  - Channel Utilization
  - FPGA Size
  - Routing, Logic, and Total Area
  - Power consumption
  - Channel Width
- Simulation of generated FPGAs
  - Leakage Power
  - Total Power
  - Area
  - Energy/Op

Contributions: FPGA Architecture Re-examination

- Thorough design space exploration of FPGA architectures across different knobs
- Recommendations for architecture parameters for ultra-low power FPGA design
- Both CAD- and simulation-based exploration
- Simulated comparisons of proposed architectures w/ current commercial and academic FPGA architecturs

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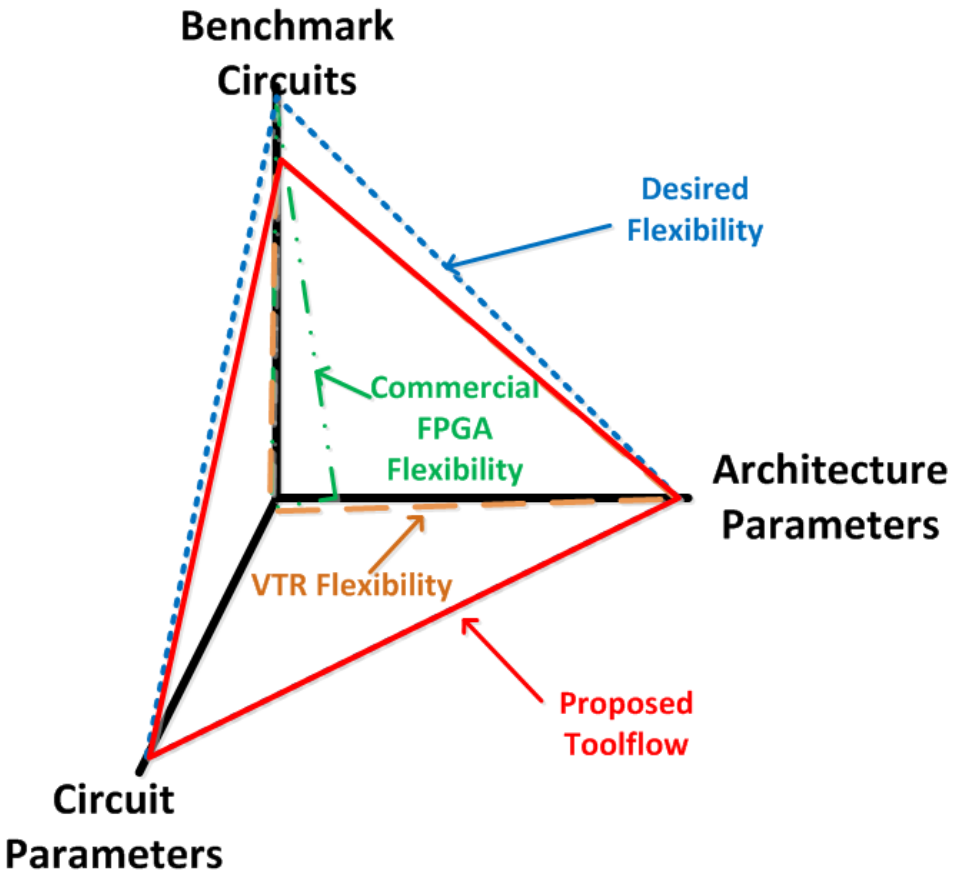
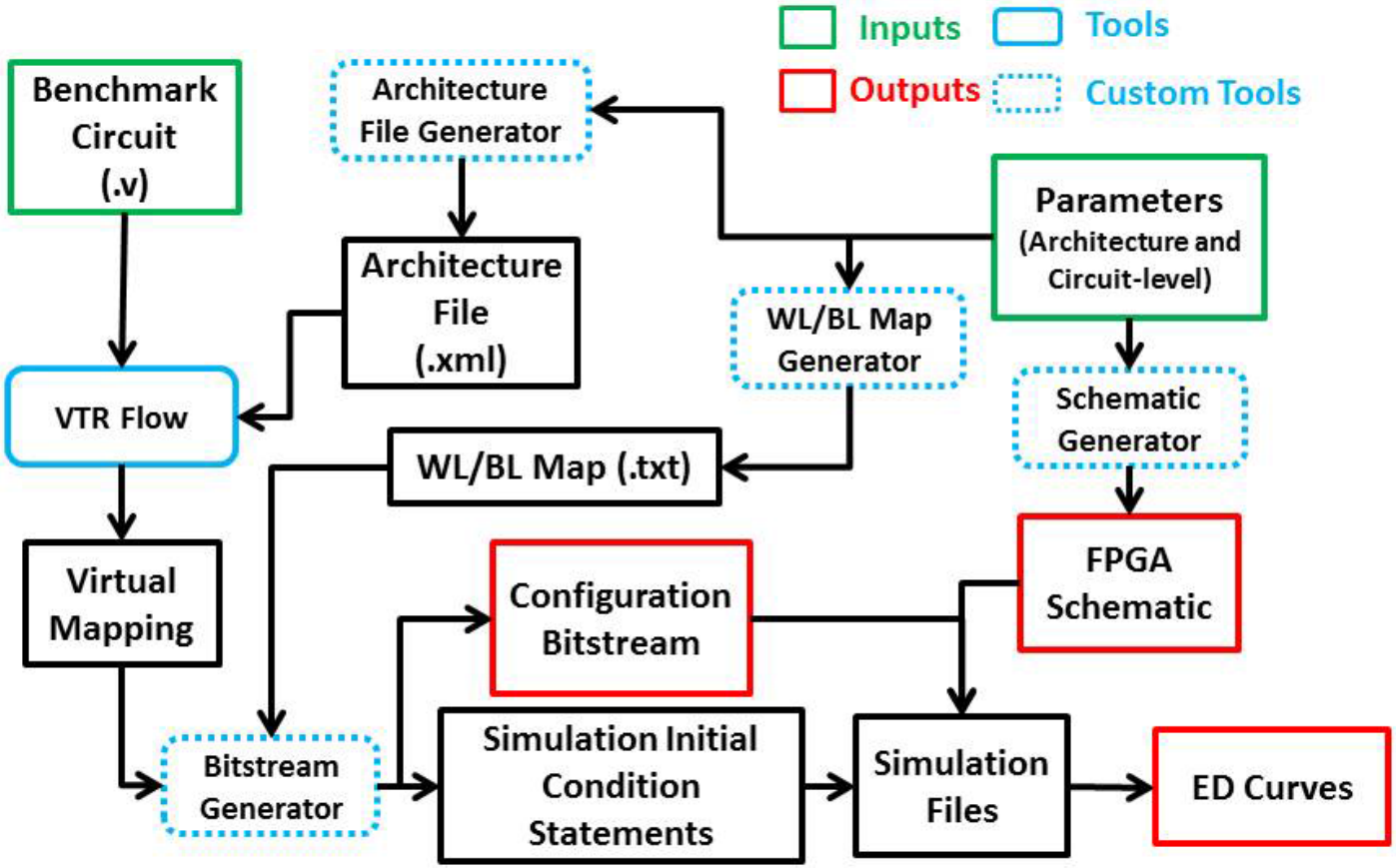
Motivation: RCGC

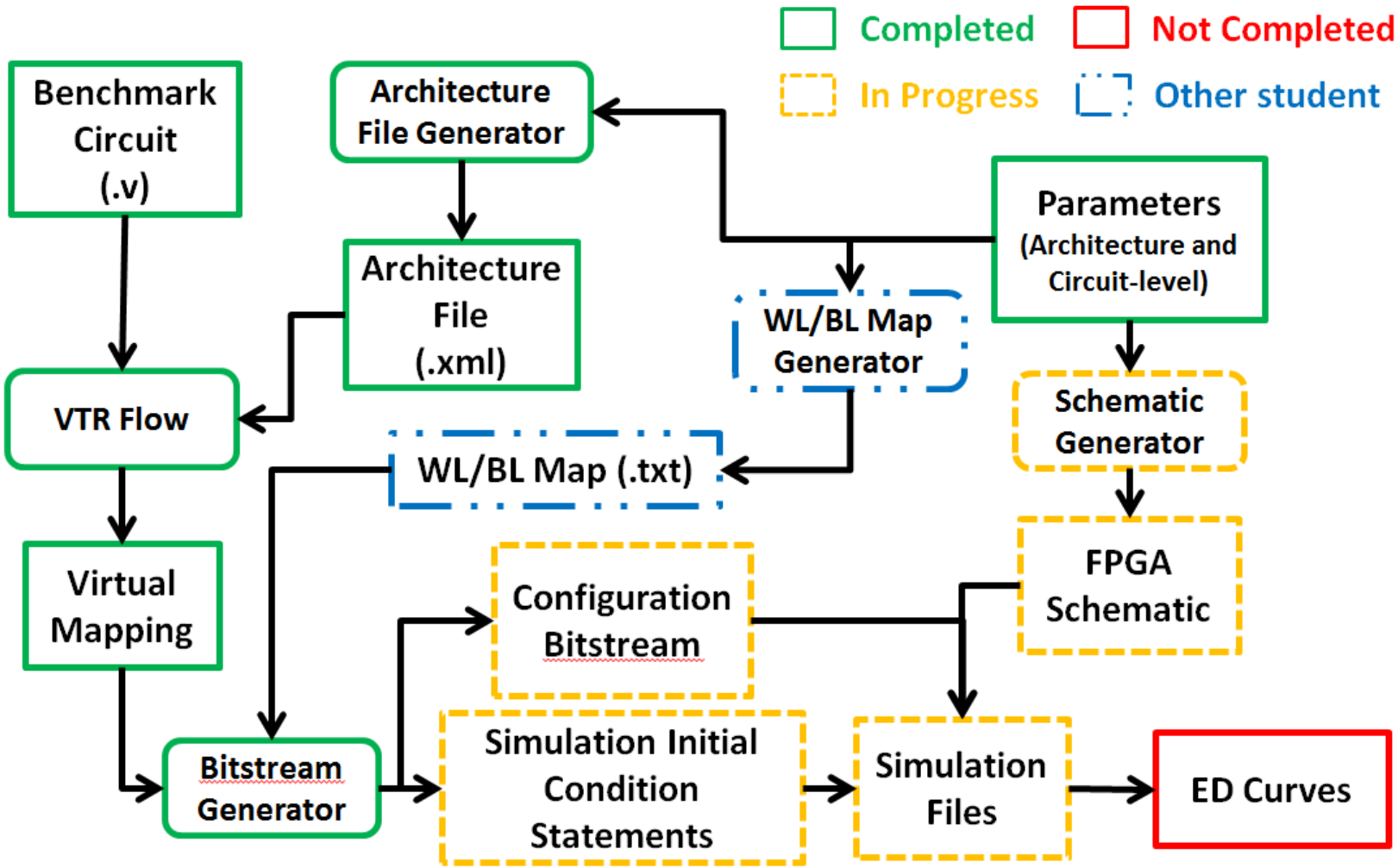


- **Research Question:** How can we extend available FPGA mapping tools to incorporate circuit-level parameters and configuration?

Approach: RCGC



Current Progress: RCGC



Contributions: RCGC

- Generates FPGA schematic from set of circuit-level and architectural parameters
- Enables rapid design space exploration (circuit-level & architecture)
- Generates configurations for custom-FPGAs
  - Initial conditions and configuration bitstream
- Enables architectural and circuit-level co-optimizations for full custom-FPGA

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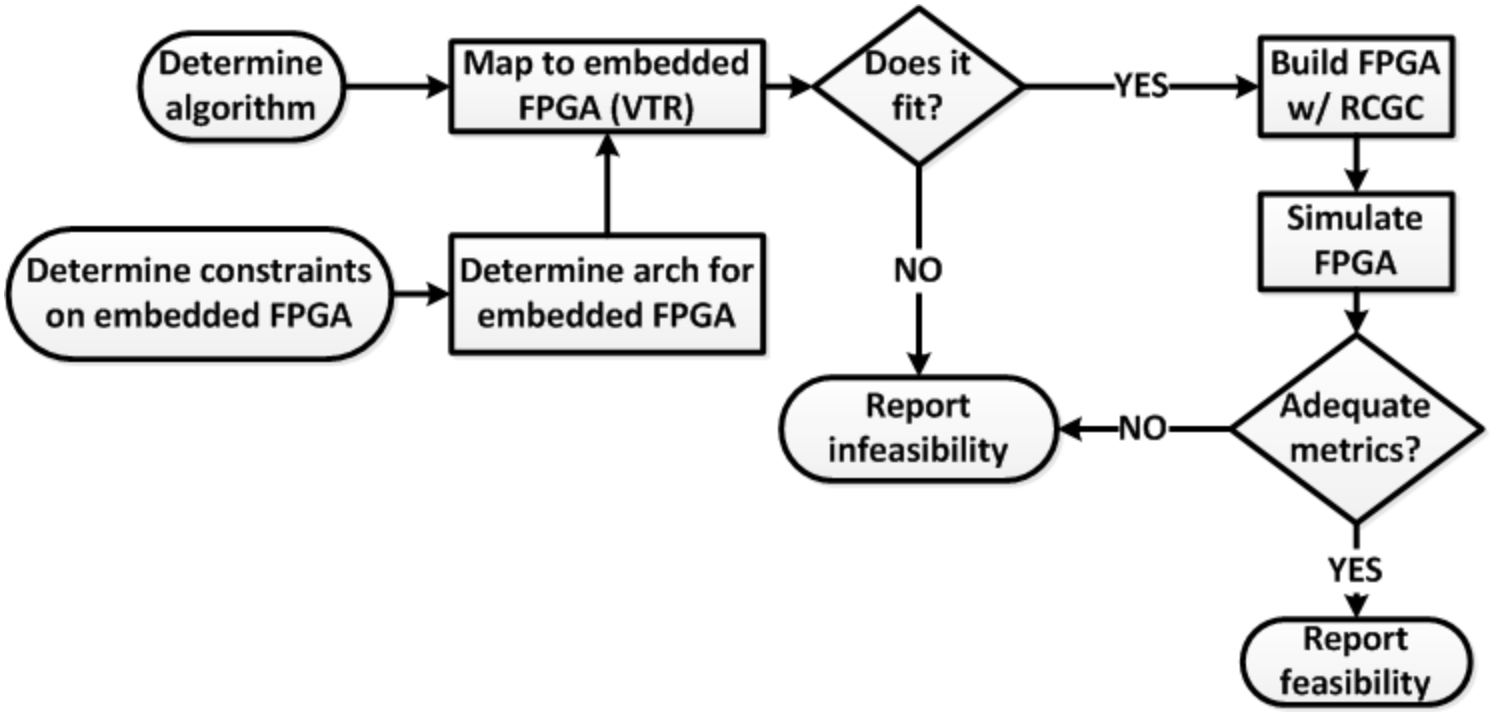
Motivation: Embedded FPGAs in ULP SoCs

- **Problem:** ULP SoCs are effective, low-power solutions, but are inflexible and costly to update

- **Research Question:** Can embedding FPGA fabric in ULP SoCs improve flexibility while keeping the power consumption low enough to maintain ULP functionality?

Approach: Embedded FPGAs in ULP SoCs



Metrics of Importance: Embedded FPGAs in ULP SoCs

- FPGA Size
- Power Consumption
- Energy Consumption
- Testability
  - Resources necessary for node BIST

Contributions: Embedded FPGAs in ULP SoCs

- Body Sensor Node (BSN) algorithm implementations on ULP FPGA fabric
- Comparison between ASIC and FPGA implementations for BSN algorithms
- Recommendation of feasibility for FPGA implementation on ULP SoCs
- FPGA implementation of test structures for ULP SoCs

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Timeline

Research Thrust	#	Task Description	Status	Related Publications
Background	1	Characterization of Commercial LP FPGAs	March '15	[OAA2]
Circuit-Level Optimization	1	Initial Routing Switch Exploration	Completed	[OAA1]
	2	Initial Sense Amp exploration	Completed	
	3	CLB Simulations	February '15	[OAA3]
	4	5T Bitcell Testing	March '15	[OAA4] [OAA5]
	5	Revisited Routing Switch Sims	April '15	
	6	Configuration Bit Simulations	May '15	
	7	Small FPGA/Test Structure Tapeout	Summer '15	
	8	Chip Testing	December '15	
Architecture Optimization	1	Initial Architecture Exploration	Completed	
	2	Characterization of FPGA sub-circuits for VTR	August '15	[OAA6]
	3	FPGA Architecture Design Space Exploration (using VTR)	September '15	
	4	FPGA Architecture Simulations	October '15	
RCGC Toolflow	1	Finish Architecture File Generator	Completed	[OAA7]
	2	Finish Schematic Generator	February '15	
	3	Finish Bitstream Generator	Completed	
	4	Finish Toolflow Wrapper	March '15	
	5	Proof of concept simulations	April '15	
Embedded FPGA Fabric	1	Determine algorithms for embedded FPGA	December '15	[OAA8]
	2	Comparison of FPGA vs. ASIC implementations	January '16	
	3	Feasibility analysis for embedded FPGAs	February '16	

Publications

Completed:

1. Oluseyi A. Ayorinde and Benton H. Calhoun. 2013. “Circuit optimizations to minimize energy in the global interconnect of a low-power FPGA (Poster).” In Proceedings of the ACM/SIGDA international symposium on Field Programmable Gate Arrays (FPGA '13). ACM, New York, NY, USA, 277-277.

Planned:

2. Dynamic power consumptions in commercial ULP FPGAs
3. Using FPGA-style Local Interconnect in CLBs for Low-Power FPGAs
4. Exploring routing switch topologies for ULP FPGA interconnects
5. Configuration Bits for ULP FPGAs
6. A new architecture for Sub-mW FPGAs
7. RCGC: A toolflow for generating custom FPGA schematics and configurations
8. Feasibility Analysis of Embedded FPGAs for ULP SoCs

High Level Impact

Current State

- Limited options for ULP FPGAs
- Inability to configure custom-FPGAs
- Infeasible for FPGA-level design space exploration
- Inflexibile ULP SoCs

Future State

- In-depth circuit and architectural exploration of ULP FPGA fabrics
- Recommendations for FPGAs as sole, low-cost solutions for low power sensors
- RCGC – enabling rapid, thorough design space exploration
- Feasibility analysis of embedded FPGAs in ULP SoCs

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10. Guy Lemieux and David Lewis. 2001. Using sparse crossbars within LUT. In Proceedings of the 2001 ACM/SIGDA ninth international symposium on Field programmable gate arrays (FPGA '01), Martine Schlag and Russell Tessier (Eds.). ACM, New York, NY, USA, 59-68.
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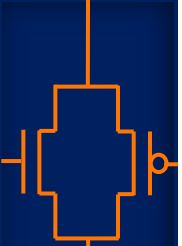


Thank you!

Backup Slide: Prior Work in ULP FPGA Sub-Circuits

- Anderson et al [9] – Interconnect routing switches
  - Lower power by adding sleep modes to routing buffers
- Grossmann et al [7] – Compared configuration bit topologies
  - Suggested 6T latches (no ratio'd circuits)
- Ryan et al [6] – Introduced mini-FPGA CLB topology
- Tuan et al [8] – uses mid-oxide high-V_T devices

Backup Slide: Prior Work in FPGA Architecture Analysis

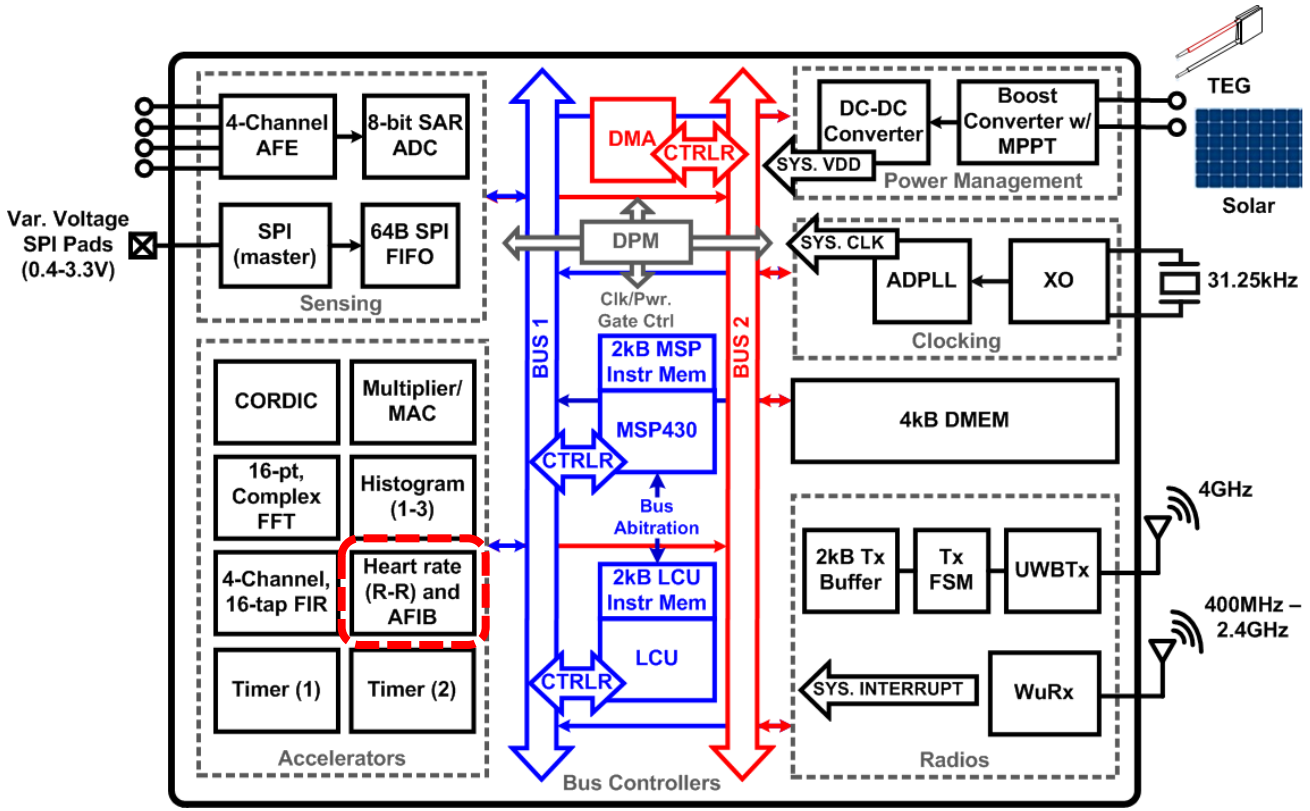
- Ahmed et al [2] – co-optimize k and N
  - K = 4-6, N = 3-10 → best area-delay product (ADP)
- Li et al [3] – optimize k, N, L, and switch topology for power minimization
  - K = 4 minimizes power, N = 12 minimizes power and power-delay product
- Jamieson et al [5] – directionality of global routing
  - High frequency: unidirectional → lower energy
  - Low frequency: bidirectional → lower energy

Backup Slide: Prior Work in Custom-FPGA toolflows

- DAGGER – Extension of Virtual Place-and-Route (VPR)
  - Designed to configure specific device
- Soni et al – Open source bitstream generation tool
  - Designed for use on existing FPGA devices
- XBits
  - Bitstream generation for custom FPGA using XML format

Backup Slide: Determining algorithms for FPGA

- Specific algorithms for different applications



Klinefelter et al ISSCC'15